AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning on page 2, line 9 and ending on page 3, line 18, with the following amended paragraph:

Accordingly, in one aspect the invention is directed to a method for fabricating an MOS device having a gate width of less than 0.3 micron that includes the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductive type wherein the interfacial layer is preferably sufficiently thin to limit parasitic capacitance of the device;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductive type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductive type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device, wherein the layer of insulator material may have an irregular surface;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

Please replace the paragraph beginning on page 4, line 3 and ending on page 4, line 18, with the following amended paragraph:

In another aspect, the invention is directed to an MOS transistor formed on a semiconductor substrate of a first conductivity type that includes:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges

from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of the second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

Please replace the paragraph beginning on page 6, line 1 and ending on page 6, line 20, with the following amended paragraph:

Subsequently, high dielectric constant layer 110 and electrically conductive layer 120 are formed on interfacial layer 105. The high dielectric constant layer 110 preferably comprises material that is selected from Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x preferably ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s preferably

ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t preferably ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof. Typically, the high dielectric constant layer will have a thickness that ranges from about 4 nm to 12 nm and preferably from about 5 nm to 10 nm. The high dielectric constant layer will form the gate oxide layer. The particular high dielectric constant materials employed with the present invention allows for a thicker gate oxide layer to be formed, resulting in less stringent requirements on gate etching selectivity during the fabrication process. In addition, it is believed that during operation of the MOS transistors, the devices will exhibit a higher transconductance parameter. Further, since Ta has already been used in MOS fabrication, Ta_2O_5 containing gate oxides are expected to be compatible with the materials in the other MOS materials. The high dielectric constant film can be fabricated by conventional means including, for example, LPCVD, PECVD, ECR CVD, UVCVD, and reactive sputtering.